ABSTRACT

A ferroelectric memory has a plurality of memory cells each having a transistor and a ferroelectric capacitor arranged in a matrix. Plate lines run in the word line direction above the ferroelectric capacitors of memory cells adjacent to each other in the word line direction among the plurality of memory cells. Bit line contacts each for connecting a bit line and an active region of the transistor are placed in regions between the plate lines adjacent to each other in the bit line direction and between the ferroelectric capacitors adjacent to each other in the word line direction. Cuts are formed at positions of the plate lines near the bit line contacts. The active regions of the transistors of the plurality of memory cells extend in directions intersecting with the word line direction and the bit line direction.